IN THE CLAIMS

Please amend the following claims.

1. (Amended) A method of forming a passivation layer on a semiconductor substrate, said method comprising the steps of:

forming a first dielectric layer over a metal interconnect layer on a semiconductor substrate, said metal interconnect layer including a bond pad and a metal member spaced apart from said bond pad by a gap, said first dielectric layer formed over said bond pad and said metal member and in said gap, wherein said first dielectric layer is at least as thick as said metal layer and said gap between said bond pad and said metal member is completely filled by said first dielectric layer; [and]

forming a second dielectric layer over said first dielectric layer [, wherein said second dielectric layer is hermetic and has a larger dielectric constant than said first dielectric layer];

forming an opening to expose the top surface of said bond pad, wherein the sidewalls of said opening expose the edges of said second dielectric layer and said first dielectric layer; and

forming a conducting barrier layer over said second dielectric layer, over sidewalls of said opening, and over said exposed top surface of said bond pad to form a continuous seal.

2. (Amended) The method of claim 1 wherein said second dielectric layer and said barrier layer are resistant to moisture penetration [first dielectric layer is at least as thick as said metal layer].

5. (Amended) The method of claim 1 wherein said barrier layer comprises a lower titanium layer and an upper nickel-vanadium layer [second dielectric layer is thinner than said first dielectric layer].

6. (Amended) A method of forming a hermetically sealed integrated circuit, said method comprising the steps of:

forming a first dielectric layer over [on a top surface of] a bond pad on a semiconductor substrate;

forming a second dielectric layer over [on] said first dielectric layer;

forming an opening [through said second dielectric and said first dielectric so as] to expose the [said] top surface of said bond pad, wherein the sidewalls of said opening expose the edges of said second dielectric layer and said first dielectric layer;

forming [depositing] a conducting barrier layer [on] over said second dielectric layer, over sidewalls [the sides] of said opening, and [on] over said exposed top surface of said bond pad to form a continuous seal, wherein said second dielectric layer and said barrier layer are resistant to moisture penetration, and

forming a bump on said barrier layer in said opening.

7. (Amended) The method of claim 6 wherein said first dielectric layer comprises silicon dioxide [second dielectric layer and said barrier layer are resistant to moisture penetration].

8. (Amended) The method of claim 6 [7] wherein [said first dielectric layer comprises silicon dioxide and] said second dielectric layer comprises silicon nitride.

9. (Amended) The method of claim 6 wherein said [conductive] barrier layer comprises a lower titanium layer and an upper [a top] nickel-vanadium layer.

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10. (Amended) The method of claim 6 wherein said bump is formed by electroplating [plating].

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11. (Amended) A method of forming a low interconnect capacitance wafer passivation, said method comprising the steps of:

forming a metal interconnect layer having a first member spaced apart from a second member by a gap;

forming a first dielectric layer over said first and second members and in said gap, wherein said first dielectric layer is at least as thick as said metal layer and said gap between said members is completely filled by said first dielectric layer;

forming a second dielectric layer over said first dielectric layer, wherein second dielectric layer has a larger [higher] dielectric constant than said first dielectric layer;

forming an opening [through said second dielectric and said first dielectric] to expose the top surface of at least one of said spaced apart members, wherein the sidewalls of said opening expose the edges of said second dielectric layer and said first dielectric layer;

forming a conducting barrier layer [metal on] over said second dielectric layer, over [the] sidewalls of said opening, and over [the] said exposed top surface of [said] at least one of said spaced apart members to form a continuous seal, wherein said second dielectric layer and said barrier layer are resistant to moisture penetration, and

forming a contact on said barrier layer [metal] in said opening.

12. (Amended) The method of claim 11 further comprising the step[s] of:

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[after forming said second dielectric and prior to forming said barrier layer,] forming a third dielectric layer over said second dielectric layer prior to forming an opening to expose the top surface of at least one of said spaced apart members.

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14. (Amended) The method of claim 13 wherein said bump is formed by electroplating [plating].

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20. (Amended) The method of claim 11 wherein said barrier layer comprises a lower titanium layer and an upper nickel-vanadium layer.